



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

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of

3

Complete if Known

Application Number	10/632,431
Filing Date	July 31, 2003
First Named Inventor	Hong Wang
Art Unit	2181
Examiner Name	MOLL, JESSE R
Attorney Docket Number	42P15449

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.†	Document Number	Publication Date Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code* (if known)			
JM		US-2004/0154019 A1	08-05-2004	Aamodt et al.	
JM		US-2005/0055541 A1	03-10-2005	Aamodt et al.	
JM		US-2004/0154012 A1	08-05-2004	Wang et al.	
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FOREIGN PATENT DOCUMENTS

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Date
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07/25/2006

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*Applicant's unique citation designation number (optional). *See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. *Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). *For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. *Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. *Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (w/1) 08/11/2003.

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T‡
JM		H. Akkary and M. Driscoll, "A Dynamic Multithreading Processor", In <i>Micro-31</i> , Proceedings of the 31st Annual International Symposium on Microarchitecture, 30 Nov.-2 Dec. 1998 Page(s):226 - 236.	
JM		J. G. Steffan, C. B. Colohan, A. Zhai, and T. C. Mowry, "A Scalable Approach to Thread-level Data Speculation", In <i>ISCA-27</i> , Proceedings of the 27th Annual International Symposium on Computer Architecture, June 2000, pages 1-12.	
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JM		V. Krishnan and J. Torrellas, "The Need for Fast Communication in a Hardware-Based Speculative Chip Multiprocessors", in <i>PACT-99</i> , Proceedings for the 1999 International Conference on Parallel Architectures and Compilation Techniques, Oct. 1999, page 24.	
JM		C. K. Luk, Tolerating Memory Latency through Software-Controlled Pre-Execution in Simultaneous Multithreading Processors, In <i>28th ISCA</i> , International Symposium on computer Architecture, June 2001, page 24.	
JM		T. Moshovos, D. Pnevmatikatos, A. Baniyasadi, "Slice Processors: An Implementation of Operation-Based Prediction", Proceedings of the 15th Annual International Conference on Supercomputing, Italy, June 2001, pages 321-334.	

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JM		<u>Speculative Precomputation on Chip Multiprocessors</u> , Jeffery A. Brown, Hong Wang, George Chrysos, Perry H. Wang, John P. Shen, at the <i>6th Workshop on Multithreaded Execution, Architecture, and Compilation (MTEAC-6)</i> , November, 2002.	
JM		M. Annavaram, J. Patel, E. Davidson. "Data Prefetching by Dependence Graph Precomputation". In <i>28th Annual International Symposium on Computer Architecture</i> , July 2001.	
JM		J. Collins, D. Tullsen, H. Wang, J. Shen, "Dynamic Speculative Precomputation". In <i>Micro 34</i> , Proceedings of the 34th Annual International symposium on Microarchitecture, December 2001, pages 306-317.	
JM		H. Wang, P. Wang, R. D. Weldon, S. Ettinger, H. Saito, M. Girkar, S. Liao, J. Shen. "Speculative Precomputation: Exploring the use of Multithreading for Latency". In <i>Intel Technology Journal</i> , Volume 6, Issue on Hyper-threading, February 2002.	
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